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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/752,116	01/06/2004	Ruei-Chin Luo	N1085-00194 [TSMC2003-045	2813

54657 7590 04/05/2006

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EXAMINER	
SIEK, VUTHE	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 04/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/752,116	LUO ET AL.
	Examiner	Art Unit
	Vuthe Siek	2825

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 January 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *6* is/are allowed.

6)☒ Claim(s) *1-5 and 7-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/752,116 filed on 1/24/2006.

Claims 1-11 remain pending in the application.

Specification

2. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

3. The abstract of the disclosure is objected to because the abstract contains language that is not relevant to description of the disclosure. Therefore, phrases: "It is emphasized that...to interprete or limit the scope or meaning of the claims." should be deleted. Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-5 and 7-11 are rejected under 35 U.S.C. 103(a) as being obvious over Gowni et al. (6,295,627 B1) in view of Chun et al. (US 2005/0071693 A1).

6. As to claim 1, Gowni et al. teach a method and apparatus automated design of memory devices comprising an advanced graphical user interface, a compiler interface (memory compiler) and a design database (Fig. 1) for designing an integrated circuit design including a peripheral circuit, a plurality of semi-custom control logic blocks and a memory array depending on user input parameters of leaf cells (Fig. 2; summary). The advanced graphical user interface is configured to allow a user to rearrange a memory array architecture by selecting one or more of a plurality of lower level leaf cells by changing a parameter selected from the group consisting of array size, defect rate, line width, line spacing, line length, gate width, transistor spacing, gate length, transistor length, resistivity, capacitance, and other physical and/or electrical device parameters (voltages, currents and powers) (col. 3, lines 22-31). By semi-custom, it means that the control logic blocks, and in general any peripheral circuitry, are automatically synthesized and/or characterized, based on lower level cell parameters of the memory array device. The parameters may be specified by user input or by the technology file utilized by the compiler interface. The semi-custom approach helps achieve optimal circuit area and performance to match with physical requirements of the compiled array (col. 6 line 59 to col. 7 line 20). Accordingly, Gowni et al. teach an advanced graphical user interface and memory compiler for designing an integrated circuit including a memory array and semi-custom of control logic blocks based user input parameters. Gowni et al. do not teach an integrated circuit design including a power management

unit to controlling a supply voltage. Chun et al. teach an integrated circuit design that includes a power management unit to controlling a supply voltage within a data processing system by providing a voltage control signal, where the data processing system including a plurality of processors that utilize different supply voltages including ultra-low power (0013-0017, 0023, 0038, 0039, 0044, 0046). By integrating a power management unit within an integrated circuit design, different values for the supply voltages can be used depending on the design of the data processing system (0023). The power management unit is able to change supply voltages faster during operation of the data processing system. This is accomplished through a compact interface by using voltage control signals (0038). Therefore, integrating the power management unit as taught by Chun et al. in the integrated circuit design that includes a memory array as taught by Gowni et al. would have obvious to practitioners in the art at the time the invention was made because the integrated power management unit would be compacted and is able to change supply voltages faster as expected during operation of the integrated circuit design that includes memory devices and other portions that used different voltage values.

7. As to claim 10, remarks set forth in rejecting claim 1 equally apply in rejecting claim 10 because similar claimed limitations. In addition, Giowni et al. teach an advanced graphical user interface and a memory compiler, where the graphical user interface inherently includes at least one region for selection of parameters that obviously includes an ultra-low power feature, when synthesizing an integrated circuit design by integrating a power management unit as taught by Chun et al. The

synthesized integrated circuit design that includes a power management unit would be compacted and able to change supply voltages faster as expected during operation of the integrated circuit design that includes memory devices and other portions that used different voltage values.

8. As to claim 2, Giowni et al. teach a memory interface (memory compiler, Fig. 1) that is adapted to create a design for at least one of (i) a static random access memory (SRAM), (ii) a read only memory (ROM), (iii) and embedded flash memory, or (iv) a single transistor random access memory (col. 4 lines 9-26).

9. As to claim 3, Chun et al. teach a power management unit that controls supply voltage within an integrated circuit design that requires less power and conserves power (reduce leakage power, 0002, 0023).

10. As to claims 4, Giowni et al. teach a method and apparatus for generating a design (memory array), layout, schematic, netlist, abstract or other equivalent circuit representations for a memory based on user input parameters and leaf cells. Using the leaf cells provided a design database is generated from the user inputs. The memory design includes a peripheral circuit. The parameters include line width, line spacing, line length, gate width, transistor spacing, gate length, transistor length, resistivity, capacitance, and/or other physical or electrical device parameters (power, timing) (see summary). Giowni et al. do not teach a circuit design including a power management unit adapted to provide a first control voltage power supply adapted to provide to a circuit peripheral to a memory cell array and to provide a second control voltage power supply adapted to provide power to the memory cell area. Chun et al. a power

management unit that provides a first control voltage and second control voltage power supply (0023, 0028) to change supply voltages faster of the integrated circuit design including different processors or other portions. The different power supply voltages could be zero, low or high voltages depending on design application. In order to provide different power supply voltages, different control power supply voltages are provided (Fig. 1, VCONTROL 1, STANDBY 1, STANDBY 2, VCONTROL 2). Therefore, integrating the power management unit having control voltage power supply (first and second controls) as taught by Chun et al. into the integrated design that includes memory cell array and a peripheral circuit as taught by Giowni et al., would have been obvious to practitioners in the art the claimed limitation because different control voltage power supplies (first and second) would expect the peripheral circuit receive appropriate voltage as required (first voltage value) and the memory cell array also receive proper voltage as required by design application.

11. As to claim 5, remarks set forth in rejecting claim 4 equally apply because Chun et al. teach providing first control supply voltage design and second control supply voltage design, where the second control voltage supply is a separate voltage supply with respect to the first control voltage power supply (Fig. 1).

12. As to claim 7, Chun et al. teach a voltage supply and control signal (Fig. 1).

13. As to claim 8, Chun et al. teach the voltage supply is a variable voltage supply which is used to provide a substantially zero voltage (0023, 0028).

14. As to claim 9, Chun et al. teach different control voltage supply at different levels (low, high, zero voltage) (read as a variable voltage supply) (0023, 0024, 0027, 0028).

The different levels of control voltage supply are provided to different portions of circuit design depending on how much voltage each the portions of the circuit design needed as required based on their design application. Integrating the different control voltage supply as taught by Chun et al. in the circuit design including memory cell array and peripheral circuit as taught by Giowni et al., it would have obvious to practitioners in the art at the time the invention was made the claimed limitations that the second variable control voltage supply allowing the second control voltage supply to operate in a minimum voltage level and to have zero voltage in static mode because by instantly controlling different levels as desired the circuit design would economically consume power, thereby this would be cost effective.

15. As to claim 11, remarks set forth in claims 1 and 10 equally apply because it would have obvious to practitioners in the art to create an electronic circuit using the process of claim 1.

Allowable Subject Matter

16. Claim 6 is allowed over the prior art of record. The prior art of record does not teach or fairly suggest providing the control voltage supply of the memory peripheral circuit with a netlist identifier which is unique with respect to a netlist identifier for the control supply voltage of the memory cell.

Remarks

17. Remarks have been considered, but they are not persuasive. Gowni et al. teach a set of user inputs describing parameters of the layout is acquired through a graphical user interface (GUI). Based on the user inputs, or at least a subset thereof, one or more

leaf cells is/are generated. Then using the leaf cells, a design database for the layout is generated from the user inputs (col. 2 lines 52-67, col. 3 lines 1-5). An advanced user graphical interface configured to allow a user to rearrange a memory array architecture by selecting one or more of a plurality of lower level leaf cells is provided. The user may rearrange the memory array architecture by changing a parameter selected from the group consisting of array size, defect rate, line width, line spacing, line length, gate width, transistor spacing, gate length, transistor length, resistivity, capacitance, and other physical and/or electrical device parameters. The electrical device parameters include power supply. Thus, when ultra low power is needed and used or not, it would have been obvious to practitioners in the art to have included a user-selectable option to selectively or de-selectively allow enablement or disablement of an ultra low power feature. The selection or de-selection of ultra low power would generate or synthesize a circuit design accordingly to design requirements (power consumption). Examiner disagrees with applicants that Chu does not suggest a plurality of processors utilize different supply voltage. Chu teaches a voltage regular, a voltage control signal, and a standby signal are shared by multiple processors, where the voltage control signal module ensure the supply voltage is changed only when the change is appropriate for all processors sharing the same voltage regulator. In addition, the power management unit as taught by Chu has a voltage regulator supplying an independently controlled supply voltage to each processor. These suggest that each processor may have used different supply voltage (0002, 0013, 0019, 0023, 0027, 0028, 0038, 0039, 0044, 0046).

Thus, the combination of teachings would render the claim limitations obvious to practitioners in the art.

18. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vuthe Siek whose telephone number is (571) 272-1906.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on (571) 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vuthe Siek

VUTHE SIEK
PRIMARY EXAMINER